REMARKS

Claims 1, 4-10, 12, 15-19 and 22-25 are rejected. Claims 1, 4-10, 12, 15-19 and 22-25 are currently pending. Applicants respectfully request further examination and reconsideration in view of the remarks set forth below. Applicants believe that the amendments herein to the patent application do not add new matter to it.

35 U.S.C. §103 Rejections

Claims 1, 4, 5 and 8 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over McCloghrie et al., U.S. Patent No. 6,920,112 (hereinafter McCloghrie) in view of DeMars et al., U.S. Patent No. 7,088,739 (hereinafter DeMars), Joao, U.S. Patent No. 5,961,332 (hereinafter Joao), and Bestler et al., U.S. Patent No. 5,680,457 (hereinafter Bestler). Claims 10, 15, 16, 19 and 22-25 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over McCloghrie in view of Genrich, U.S. Patent No. 5,596,609 (hereinafter Genrich), Schueler, U.S. Patent No. 5,682,034 (hereinafter Schueler), and Pase, U.S. Patent No. 6,128,639 (hereinafter Pase). Claim 9 is rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over the combination of McCloghrie, DeMars, and Bestler as applied to Claim 1, and further in view of Dean, U.S. Patent No. 6,442,585 (hereinafter Dean). Claims 6 and 7 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over the combination of McCloghrie, DeMars, and Bestler as applied to Claim 1, and further in view of Chen et al., U.S. Patent No. 6,658,006 (hereinafter Chen). Claim 17 is rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over the combination of McCloghrie, Genrich, and Schueler as applied to Claim 10, and further in view of Chen. Claim 18 is rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over the combination of McCloghrie, Genrich, and Schueler as applied to Claim 10, and further in view of Chen and Westphal, U.S. Patent No. 6,651,052 (hereinafter Westphal). Claim 12 is rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over the combination of McCloghrie, Genrich, and Schueler as applied to Claim 10, and further in view of Dean.

Claims 1 and 4-9

Applicants respectfully direct the Examiner to newly amended independent Claim 1 (emphasis added):

> A network device comprising:
>
> a first central processing unit (CPU), wherein said first CPU is integrated within said network device;
>
> an input interface comprising a microcontroller for controlling operation of said input interface, said input interface is coupled to said first CPU, said input interface for receiving a plurality of packets, said input interface comprising a plurality of input ports wherein at least one input port of said plurality of input ports is configured to sample at least one input packet and transmit a sampled input packet to said first CPU, said microcontroller of said input interface is coupled to said plurality of input ports, wherein at least one input port of said plurality of input ports comprises a countdown register, and wherein said input port is configured to sample a packet according to said countdown register, said countdown register operates by counting incoming packets;
>
> a second CPU that is integrated within said network device;
>
> an output interface comprising a microcontroller for controlling operation of said output interface, said input interface is coupled to said second CPU, said output interface for transmitting a plurality of packets, said output interface comprising a plurality of output ports wherein at least one output port of said plurality of output ports is configured to sample at least one output packet and transmit a sampled output packet to said second CPU, said microcontroller of said output interface is coupled to said plurality of output ports, wherein at least one output port of said plurality of output ports comprises a countdown register, and wherein said output port is configured to sample a packet according to said countdown register, said countdown register operates by counting outgoing packets; and
>
> wherein a packet can travel between said input interface and said output interface.

Applicants respectfully contend that McCloghrie, DeMars, Joao and Bestler, alone or in combination, fail to teach or suggest the above recited combination of elements as recited in amended independent Claim 1. For example, Applicants respectfully assert that McCloghrie, DeMars, Joao and Bestler, alone or in combination, do not teach or suggest "an input interface comprising a microcontroller for controlling operation of said input interface, . . . , said microcontroller of said input interface is coupled to said plurality of input ports" as recited in amended Claim 1. In addition, Applicants respectfully contend that McCloghrie, DeMars, Joao and Bestler, alone or in combination, fail to teach or suggest "an output interface comprising a microcontroller for controlling operation of said output interface, . . . , said microcontroller of said

output interface is coupled to said plurality of output ports" as recited in amended Claim 1. Applicants respectfully assert that McCloghrie, DeMars, Joao and Bestler are silent with regard to a microcontroller. Therefore, since McCloghrie, DeMars, Joao and Bestler, alone or in combination, fail to teach or suggest elements as recited in amended independent Claim 1, Applicants respectfully submit that amended independent Claim 1 overcomes the rejections under 35 U.S.C. §103(a), and is thus in condition for allowance.

With respect to Claims 4-9, Applicants respectfully point out that Claims 4-9 depend from allowable amended independent Claim 1 and recite further patentable subject matter.

Claims 10, 12 and 15-18

Applicants respectfully direct the Examiner to newly amended independent Claim 10 (emphasis added):

> A method of sampling a packet comprising:
>
> receiving a plurality of packets at an input network circuit of a network device, said input network circuit comprising a plurality of input ports, said input network circuit comprising a microcontroller for controlling operation of said input network circuit, said microcontroller of said input network circuit is coupled to said plurality of input ports;
>
> sampling at least one input packet at an input port of said plurality of input ports, wherein said sampling comprises using a countdown circuit;
>
> transmitting at least one sampled input packet to a processor of said network device, wherein said processor is integrated within said network device;
>
> transmitting at least one packet from said input network circuit to an output network circuit of said network device over a switching fabric of said network device, said output network circuit comprising a plurality of output ports, said output network circuit comprising a microcontroller for controlling operation of said output network circuit, said microcontroller of said output network circuit is coupled to said plurality of output ports, wherein said input network circuit and said output network circuit feed into said processor;
>
> sampling multiple output packets simultaneously at said plurality of output ports, wherein said sampling comprises using a plurality of countdown circuits, wherein each of said plurality of output ports comprises one of said plurality of countdown circuits; and
>
> transmitting said multiple sampled output packets to said processor and a second processor.

Applicants respectfully contend that McCloghrie, Genrich, Schueler and Pase, alone or in combination, fail to teach or suggest the above recited combination of elements

as recited in amended independent Claim 10. For example, Applicants respectfully assert that McCloghrie, Genrich, Schueler and Pase, alone or in combination, do not teach or suggest "said input network circuit comprising a microcontroller for controlling operation of said input network circuit, said microcontroller of said input network circuit is coupled to said plurality of input ports" as recited in amended Claim 10. Furthermore, Applicants respectfully contend that McCloghrie, Genrich, Schueler and Pase, alone or in combination, fail to teach or suggest "said output network circuit comprising a microcontroller for controlling operation of said output network circuit, said microcontroller of said output network circuit is coupled to said plurality of output ports" as recited in amended Claim 10. Applicants respectfully assert that McCloghrie, Genrich, Schueler and Pase are silent with regard to a microcontroller. Therefore, since McCloghrie, Genrich, Schueler and Pase, alone or in combination, fail to teach or suggest elements as recited in amended independent Claim 10, Applicants respectfully submit that amended independent Claim 10 overcomes the rejections under 35 U.S.C. §103(a), and is thus in condition for allowance.

With respect to Claims 12 and 15-18, Applicants respectfully point out that Claims 12 and 15-18 depend from allowable amended independent Claim 10 and recite further patentable subject matter.

Claims 19 and 22

Applicants respectfully direct the Examiner to newly amended independent Claim 19 (emphasis added):

> A network device for sampling a packet comprising:
>
> processing means, wherein said processing means is integrated into said network device;
>
> input interface means for receiving a plurality of packets over a network, said input interface means comprising a plurality of input means for sampling at least one packet, said input interface means comprising a microcontroller for controlling operation of said input interface means, said microcontroller of said input interface means is coupled to said plurality of input means, said input interface means for transmitting a sampled incoming packet to said processing means, said input interface means coupled to said processing means;
>
> output interface means for transmitting a plurality of packets over said network, said output interface means comprising a plurality of output means for sampling multiple output packets simultaneously, said output interface means comprising a microcontroller for controlling operation of said output interface means, said microcontroller of said output interface means is coupled to said plurality of output means, said input interface means for transmitting said

multiple sampled output packets to said processing means and a second processing means, wherein each of said plurality of output means comprises a countdown means, wherein at least one input means of said plurality of input means comprises a countdown means, and wherein said input means is configured to sample a packet of said plurality of packets according to said countdown means; and

switching means coupled to said input interface means and said output interface means, said switching means for transmitting a packet between said input interface means and said output interface means.

Applicants respectfully contend that McCloghrie, Genrich, Schueler and Pase, alone or in combination, fail to teach or suggest the above recited combination of elements as recited in amended independent Claim 19. For example, Applicants respectfully assert that McCloghrie, Genrich, Schueler and Pase, alone or in combination, do not teach or suggest "said input interface means comprising a microcontroller for controlling operation of said input interface means, said microcontroller of said input interface means is coupled to said plurality of input means" as recited in amended Claim 19. Moreover, Applicants respectfully contend that McCloghrie, Genrich, Schueler and Pase, alone or in combination, fail to teach or suggest "said output interface means comprising a microcontroller for controlling operation of said output interface means, said microcontroller of said output interface means is coupled to said plurality of output means" as recited in amended Claim 19. Applicants respectfully assert that McCloghrie, Genrich, Schueler and Pase are silent with regard to a microcontroller. Therefore, since McCloghrie, Genrich, Schueler and Pase, alone or in combination, fail to teach or suggest elements as recited in amended independent Claim 19, Applicants respectfully submit that amended independent Claim 19 overcomes the rejections under 35 U.S.C. §103(a), and is thus in condition for allowance.

With respect to Claim 22, Applicants respectfully point out that Claim 22 depends from allowable amended independent Claim 19 and recite further patentable subject matter. Therefore, Applicants respectfully submit that Claim 22 overcomes the rejections under 35 U.S.C. §103(a), and is thus in condition for allowance for at least being dependent on an allowable base claim.

Claims 23-25

Applicants respectfully direct the Examiner to newly amended independent Claim 23 (emphasis added):

> A network device comprising:
> a first processor integrated within said network device;
> a second processor integrated within said network device;
> a switching fabric;
> an input interface coupled to said switching fabric, said input interface comprising a plurality of input ports, said input interface is coupled to said first processor, said input interface comprising a microcontroller for controlling operation of said input interface, said microcontroller of said input interface is coupled to said plurality of input ports, said input interface for sampling at least one incoming packet received at one of said plurality of input ports, wherein each of said plurality of input ports comprises a countdown register, said input interface for transmitting said sampled incoming packet to said first processor;
> an output interface coupled to said switching fabric, said output interface comprising a plurality of output ports, said output interface is coupled to said first processor and said second processor, said output interface comprising a microcontroller for controlling operation of said output interface, said microcontroller of said output interface is coupled to said plurality of output ports, said output interface for sampling multiple outgoing packets simultaneously at said plurality of output ports, wherein said sampling comprises using a plurality of countdown circuits, wherein each of said plurality of output ports comprises one of said plurality of countdown circuits, said output interface for transmitting said multiple sampled outgoing packets to said processor and a second processor;
> a computer-readable memory coupled to said input interface and said output interface; and
> wherein a packet can travel between said input interface and said output interface via said switching fabric.

Applicants respectfully contend that McCloghrie, Genrich, Schueler and Pase, alone or in combination, fail to teach or suggest the above recited combination of elements as recited in amended independent Claim 23. For example, Applicants respectfully assert that McCloghrie, Genrich, Schueler and Pase, alone or in combination, do not teach or suggest "said input interface comprising a microcontroller for controlling operation of said input interface, said microcontroller of said input interface is coupled to said plurality of input ports" as recited in amended Claim 23. Additionally, Applicants respectfully contend that McCloghrie, Genrich, Schueler and Pase, alone or in combination, fail to teach or suggest "said output interface comprising a microcontroller for controlling operation of said output interface, said microcontroller of said output interface is coupled to said plurality of output ports" as recited in amended

Claim 23. Applicants respectfully assert that McCloghrie, Genrich, Schueler and Pase are silent with regard to a microcontroller. Therefore, since McCloghrie, Genrich, Schueler and Pase, alone or in combination, fail to teach or suggest elements as recited in amended independent Claim 23, Applicants respectfully submit that amended independent Claim 23 overcomes the rejections under 35 U.S.C. §103(a), and is thus in condition for allowance.

With respect to Claims 24 and 25, Applicants respectfully point out that Claims 24 and 25 depend from allowable amended independent Claim 23 and recite further patentable subject matter. Therefore, Applicants respectfully submit that Claims 24 and 25 overcome the rejections under 35 U.S.C. §103(a), and are thus in condition for allowance for at least being dependent on an allowable base claim.

CONCLUSION

For all the reasons advanced above, Applicants respectfully submit that pending Claims 1, 4-10, 12, 15-19 and 22-25 are in condition for allowance and that action is respectfully solicited.

The Examiner is invited to contact Douglas M. Gilbert at (408) 447-4447 if the Examiner believes such action would expedite resolution of the present application.

Respectfully submitted,
MURABITO, HAO & BARNES LLP

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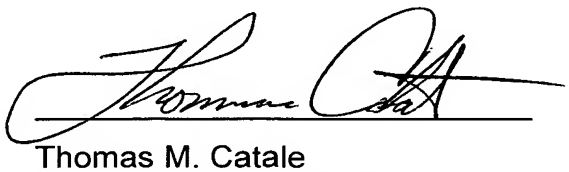

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